(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 458 385 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 91201116.0

(22) Date of filing: 10.05.91

(51) Int. Cl.[5]: H04L 27/34

(30) Priority: 18.05.90 IT 2038090

(43) Date of publication of application: 27.11.91 Bulletin 91/48

(84) Designated Contracting States: CH DE ES FR GB GR IT LI SE

(71) Applicant: SIEMENS TELECOMUNICAZIONI S.P.A.
SS. 11 Padana Superiore Km. 158
I-20060 Cassina de Pecchi (Milano)(IT)

(72) Inventor: Lo Curto, Michelangelo
Via Virgilio, 4
I-20038 Seregno (Milano)(IT)
Inventor: Salerno, Marcello
Via Bosatra, 12
I-20064 Gorgonzola, (Milano)(IT)

(74) Representative: Mittler, Enrico et al
c/o Marchi & Mittler s.r.l. Viale Lombardia, 20
I-20131 Milano(IT)

(54) Wholly digital process for the generation of multi-level modulation signals.

(57) A process for actuation of multi-level digital modulation and in particular QAM modulation by using a single microprocessor (DSP) is described.

The process calls for synchronism of all the frequencies in play and comprises an oversampling of the symbols of the 'in phase' and 'in quadrature' channels and appropriate digital filtration thereof.

A digital carrier is QAM modulated simply by selecting in string the symbols belonging to said digitally filtered channels taken with their true of negated value. Said symbols are then sent to a digital/analog converter (DAC) followed by a reconstruction filter (FRIC) to obtain the corresponding QAM modulated analog carrier.

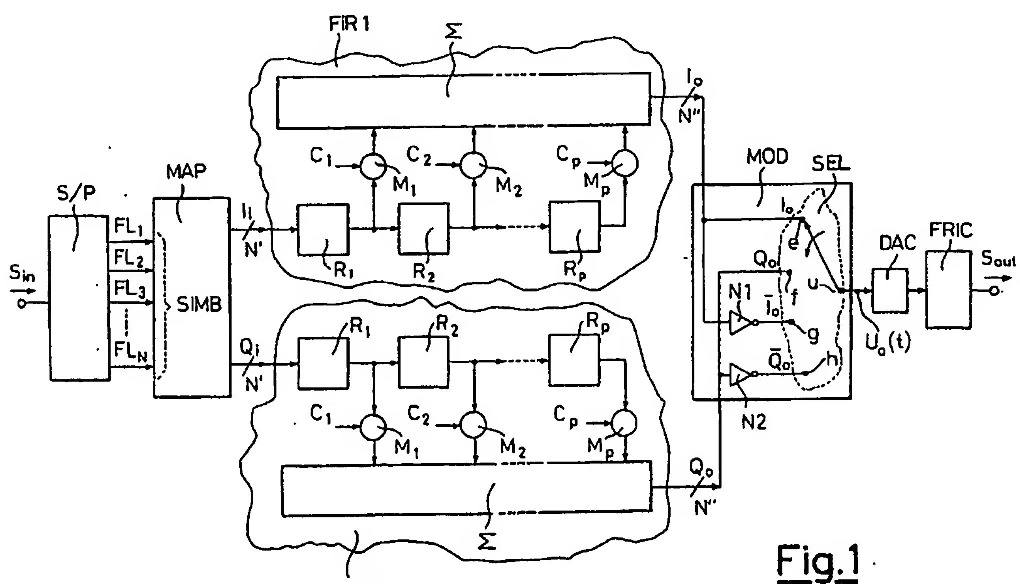


Fig.1

EP 0 458 385 A2

The present invention relates to the field of digital modulation of sinusoidal carriers and more specifically to a process for actuation of multi-level digital modulation by a digital signal processor.

In multi-level digital modulation the modulating signal is generally in the form of a flow of serial bits with a frequency of fb bits. Said flow is converted into N parallel flows of bits (N = 1,2,3....) of which the N bits present simultaneously on the N flows form words denominated symbols having a symbol frequency fs = fb/N.

Each N bit symbol can express a number of 2^N different combinations of bits. The number 2^N is termed modulation level.

For low modulation levels (2^N = 2,4,8) there is ordinarily used PSK (Phase Shift Keying) modulation which associates with each symbol one phase of a carrier.

For higher levels of modulation recourse is usually had to QAM (Quadrature Amplitude Modulation) modulation which associates with each symbol not only the phase but also the level of a carrier. The possible 2^N values of the phases and level combinations of the modulated carrier are generally represented by a constellation of points in a Cartesian plane the axes of which represent two mutually sinusoidal in quadrature carriers.

Each point of the constellation is identified by a vector which departs from the origin of the plane. The components of the vectors in relation to the Cartesian axes are obtained directly from the symbols by an operation termed 'mapping' which associates with each symbol two other symbols whose values are the above components.

The associated symbols form two flows with frequency fs termed 'in phase' channel I and 'in quadrature' channel Q respectively.

In a conventional QAM modulator the symbols of the I and Q channels are converted from digital to analog and filtered with two shaping filters to appropriately shape the spectrum of the two analog signals obtained. Said signals are then used to modulate two synchronous sinusoidal carriers in quadrature with each other. The modulated carriers are added together to obtain a single modulated carrier in the desired QAM mode.

Shaping of the above mentioned spectrum is performed by a filtration described as 'optimum' of the symbols belonging to the in phase and in quadrature channels.

In view of the foregoing a conventional QAM modulator includes the following:

- a series/parallel converter to convert the serial input flow into N parallel bit flows;
- a mapping memory to obtain the I and Q channels starting from the N parallel flows;
- two digital/analog converters for conversion of the symbols of the I and Q channels into continuous values;
- two 'optimum' analog filters placed after said converters;
- two analog multipliers to whose first inputs arrive the output signals from the 'optimum' filters, to whose second inputs arrive two sinusoidal in quadrature carriers and whose outputs are the above said amplitude modulated carriers respectively, and
- an analog adder to whose inputs arrive the outputs of the multipliers and whose output is a single QAM modulated carrier.

The conventional modulator however has a serious drawback due to the fact that the gain of the analog multipliers shows strong tolerances and is susceptible to thermal drift which introduces phase and amplitude inaccuracies in the modulated signal. The consequences of said inaccuracies are notices mainly at the higher modulation levels (N > 4).

Said shortcomings are overcome by having recourse to QAM modulators of a second type provided in a known manner completely in digital mode.

Said modulators do not require the two digital/analog converters on the I and Q channels as in the above converters because the respective symbols undergo the 'optimum' filtration directly in digital mode. The filtered symbols are also multiplied digitally by the values of the sinusoidal in quadrature carriers appropriately digitalized. The digital samples of the product are converted into analog and filtered by means of a low pass filter, termed 'reconstruction', to eliminate the unwanted spectral components and obtain the modulated sinusoidal carrier QAM.

As is known, to digitally filter signals it is first necessary to sample them with a sampling frequency fc whose value must be equal to at least twice the maximum frequency contained in the band of the signal to be sampled. In the case in question the signals to be sampled correspond to the symbols of the I and Q channels and said maximum frequency corresponds to the symbol frequency fs:

The spectrum of a sampled signal is formed of an infinite series of spectra of the signal in base band placed around whole multiples of the frequency fc constituting overall a repetition spectrum.

To further space the repeated spectra it is useful to perform an oversampling of the symbols at the

frequency fc = fs x K where K is a whole number > 2 representing the number of samples per symbol.

The value of K is selected so that the distance between two repeated spectra is broad enough for an embodiment of the reconstruction filter with a slope not overly steep of the attenuation characteristic with the frequency.

The QAM modulators of the second type have however a considerable circuit complexity due mainly to the high number of multipliers included in the digital filters placed on the I and Q channels, a number which will be greater in proportion to the accuracy of the filter and the higher the sampling frequency fc selected.

Accordingly the purpose of the present invention is to overcome the above shortcomings and indicated a process for actuation of the multi-level digital modulation which, considering the string of operation phases of a hypothetical circuit taken as a whole, allows minimisation of the number of operations necessary to complete said modulation.

The process in question shows itself to be particularly well suited to implementation by a single microprocessor specialized in real time digital signal processing (DSP).

To achieve said purposes the object of the present invention is a process for actuation of multi-level digital modulation as described in claims 1 through 5.

Another object of the invention is a device for actuation of multi-level digital modulation as described in claims 6 and 7.

The process which is the object of the invention while allowing the embodiment of a QAM modulator by means of a single DSP permits considerable circuit simplification as compared with an embodiment with conventional circuits.

Other objects and advantages of the present invention will be made clear by the detailed description given below of an example of embodiment thereof and the annexed drawings given merely as an illustrative and nonlimiting example wherein:

FIG. 1 shows a block diagram of a hypothetical QAM circuit modulator which actuates the modulation process which is the object of the present invention,

FIG. 2 shows the temporal evolution of a string of symbols developed by the circuit of FIG. 1,

FIGS. 3, 4 and 5 represent flow charts of the phases which characterize the process which is the object of the present invention provided by a digital signal processor (DSP).

With reference to FIG. 1 there is noted a series/parallel S/P converter having an input of a serial flow of S_{in} bits with frequency fb and an output N of parallel flows of bits at the frequency fs = fb/N. As stated above the bits on the N flows at the end of each individual phase of parallelization form words of N bits called symbols and having a symbol frequency fs. The N flows reach the input of a mapping memory MAP which associates with each input symbol two new symbols in output each having a number of bits N' = Integer[N/2] approximated to the nearest greater whole number.

The symbols output from the block MAP, indicated by Ii and Qi, belong to two parallel flows of bits at frequency fs which form two channels, termed 'in phase' channel I and 'in quadrature' channel Q respectively.

The symbols Ii and Qi reach the input of two identical transverse digital filters FIR1 and FIR2 respectively with 'p' taps, having a finite pulse response (FIR) similar to that of an 'optimum' transmission filter.

As mentioned above, the symbols at the input of the digital filters are sampled with a frequency of fc = fs x K.

Each of the two filters FIR1 and FIR2 is embodied in a known manner and includes a number 'p' of memory registers R1, R2, ... Rp, a number 'p' of digital multipliers M1, M2, ...Mp and an adder Z with 'p' inputs where the number 'p' will be selected in accordance with the criteria defined below.

The registers are arranged in sequence with the first R1 coinciding with the input of the respective filter FIR1 or FIR2. Each register memorizes a sample for an interval of time T = 1/fc at the end of which it transfers it to the subsequent register, delaying it by T. During each interval T the delayed samples are sent to first inputs of the multipliers M1, M2, ... Mp to second inputs of which arrive coefficients C1, C2, ... Cp, of N" bits unvarying in time. The products output from said multipliers reach the inputs of the respective adders Z which add them together at each interval T, producing at the outputs symbols of N" bits indicated by Io and Qo.

The symbols Io and Qo correspond to the symbols Ii and Qi respectively after the digital filtration.

Said symbols Io and Qo reach two distinct inputs of a modulator block MOD for modulation of two respective sinusoidal carriers digitalized together in quadrature.

This block includes two invertors N1, N2 and an electronic selector SEL with four inputs (e, f, g, h) placed in string and an output point u coinciding with the output of the block MOD.

The symbols Io reach directly the input point e of the selector SEL and the point g through the invertor

N1; the symbols Qo reach directly the input point f of the selector SEL and the point h through the invertor N2.

The selector SEL selects with timing cadence T the signal present at one of the input points in the string e, f, g, h and transfers it to the output point u. The resulting output flow from the block MOD reaches a digital/analog converter DAC of known type whose output is connected to a low pass reconstruction filter FRIC also of known type.

The signal Sout output from the filter FRIC is the output signal of the modulator circuit QAM indicated in the figures.

In operation the block MOD performs amplitude modulation of two sinusoidal carriers digitalized in quadrature with each other using as modulating signals the filtered signals Io and Qo respectively. Said carriers are not shown in the figures because, as will be clarified below, they are not really necessary.

Another function of the block MOD is the sum of the modulated carriers for obtaining a single modulated digital carrier QAM indicated by Uo(t) to be sent to the digital/analog converter DAC.

As is known, amplitude modulation of digital signals is achieved by digitally multiplying samples of the carrier signals by samples of the modulating signals.

From the explanation of the circuit of the block MOD it may however be noted that said block contains no multiplying nor adding circuits. This circuit simplification is made possible by some peculiarities of the process being discussed. More specifically:

- the two digitalized sinusoidal carriers phase shifted with each other by one fourth of a period are synchronous with the sampling frequency fc,
- the frequency fo of the two carriers is assumed equal to 1/4 of the sampling frequency fc so as to obtain four samples for each period of said carriers, and
- the carriers are sampled at their highest, lowest and null levels coinciding with the standardized levels equal to +1, -1 and 0 respectively.

According to these hypotheses the strings of samples for the two carriers, which are obtained at intervals T, are the following.

In phase carrier	+1	0	-1	0	+1	.....
In quadrature carrier	0	+1	0	-1	0	.....

the corresponding strings of symbols Io and Qo are:

Io(T)	Io(T-1)	Io(T-2)	Io(T-3)	....
Qo(T)	Qo(T-1)	Qo(T-2)	Qo(T-3)	....

the corresponding strings of samples associated with the two modulated carriers and obtained by multiplying carrier samples by modulating signal samples are:

+Io(T)	0	-Io(T-2)	0	....
0	+Qo(T-1)	0	-Qo(T-3)	....

the string of samples obtained from the sum of the two preceding strings, is:

Uo(t) = +Io(T) +Qo(T-1) Io(T-2) -Qo(T-3) ....

said samples are indicated in FIG. 1 by Io, Qo, $\overline{\text{Io}}$, $\overline{\text{Qo}}$.

As may be seen, the amplitude modulation performed by the block MOD is reduced to a choice of samples, true or negated, made on the symbols Io and Qo coming from 'in phase' and 'in quadrature' channels. This justifies what was said above concerning the fact that in reality no carrier reaches the block MOD.

Sizing of the digital filters FIR1 and FIR2 involves determination of a 'period of observation' of the input signals which correspond to the time employed by a symbol Ii or Qi to pass through the respective digital filter. This is equivalent to determination of the number M of symbols simultaneously present in the filter memory registers.

The total length of each filter, which corresponds to the number 'p' of taps, is given by the following formula:

p = M x K

where K = fc / fs is the number of samples per symbol.

The value of M depends mainly on the degree of accuracy required of the filters.

In view of the foregoing the value of K must cause a mutual spacing of the repeated spectra higher than the minimum allowed, obtained by K = 2, so as to permit ready embodiment of the reconstruction filter FRIC.

Choosing for example K = 4 and M = 4 we have:

fc = 4fs p = 16

With K = 8 and M = 4 we have:

fc = 8fs p = 32, etc.

The reconstruction filter can only be simplified by increasing the length of the digital filters. Said complication is however easy to overcome. Indeed, from the oversampling operation performed, for every value of K it is possible to make the first of the K samples per symbol equal to the value of said symbol and all the bits of the subsequent K - 1 samples equal to zero. It follows that a large part of the products inside the digital filters are null. Therefore for each filter the number of multiplications really necessary is reduced to one for each symbol time for the number M of symbols contained in the filter regardless of the value of K. Totally, considering the two filters, 2M multiplications for each symbol time. However, in view of what was said above about operation of the block MOD, it would seem possible to halve the total number of multiplications, making it M. Indeed, during one symbol time said multiplications are performed alternately on the symbols Ii or Qi.

Operation of the circuit of FIG. 1 assumes synchronism of all the frequencies in play (fb, fs, fc, fo), with:

fc = fs x K
fo = fc/4 = fs x (K/4).

This said, in the modulator of FIG. 1 the input operations for the block S/P are performed at frequency fb, the operations for the block MAP are performed at frequency fs and all the operations for the remainder of the circuit are performed at frequency fc. Consequently the modulated carrier QAM output from the block DAC consists of the discrete samples which succeed each other at frequency fc.

FIG. 2 shows the temporal evolution of the content of the registers of one of the two filters FIR1 or FIR2 without distinction (FIG. 1) in the case where K = 4, M = 4 and p = 16.

With reference to FIG. 2 there can be seen the array S1 of the multiplicative coefficients C1, ... Cp which are supplied to the corresponding second inputs of the multipliers M1, ... Mp (FIG. 1).

Opposite the array S1 there are seen five sequences indicated by S2, S3, S4, S5 and S6 aligned one under the other, each one comprising 16 samples for the symbols Ii or Qi (FIG. 1). The sequence S6 refers to a present interval of time T. The sequences S5, S4, S3, and S2 refer to time intervals indicated above by T - 1, T - 2, T - 3, T - 4.

Starting from the sequence S2 which includes samples of four complete symbols indicated by D3, D2, D1 and D0 each subsequent sequence is obtained by shifting all the samples of the previous sequence to the right with loss of the last sample and introducing on the left a new sample D4 in S6.

As may be seen, the symbols inside the sequences, in this case of K = 4, are made up of a sample of the symbol and 3 samples of all zeros.

The filtered symbols Io and Qo are obtained by multiplying at every interval T each sample of the sequence by the corresponding coefficient and adding all the products together.

Therefore, ignoring the null products, the flow of symbols indicated for example by Io will have in the various instants the following expressions:

Io(T-4) = D3xC1 + D2xC5 + D1xC9 + D0xC13
Io(T-3) = D3xC2 + D2xC6 + D1xC10 + D0xC14
Io(T-2) = D3xC3 + D2xC7 + D1xC11 + D0xC15
Io(T-1) = D3xC4 + D2xC8 + D1xC12 + D0xC16
Io(T) - D4xC1 + D3xC5 + D2xC9 + D1xC13

The flow of symbols indicated by Qo has a similar expression.

FIGS. 3, 4, 5 as stated illustrate a possible flow chart microprogramme memorised in a microprocessor for the embodiment of the modulation process in question for the circuit of FIG. 1. In view of what was said above, it is observed that the circuit of FIG. 1 is a hypothetical circuit given only for explanatory purposes. The actual implementation shown in FIGS. 3, 4 and 5 minimizes the number of operations and the number of memory registers.

As a nonlimiting example it would be possible to provide the modulation process by means of the microprocessor produced by the Analog Devices Co. under stock number ADSP-2100.

The information contained in the operating manuals of the microprocessor together with the detailed description of the flow chart shown in FIGS. 3, 4 and 5 are sufficient for those skilled in the art to provide a QAM modulator circuit of FIG. 1 in accordance with the modulation process which is the object of the invention.

Said modulator circuit in the embodiment using a microprocessor comprises:

- the microprocessor mentioned above or equivalent,
- an oscillator circuit for generation of the clock signal of the microprocessor,
- a synchronization circuit for the generation of appropriate interruption signals to send to the microprocessor, and
- the digital/analog converter DAC (FIG. 1) and the reconstruction filter FRIC (FIG. 1).

The synchronization circuit comprises an oscillator for generation of a main frequency and one or more frequency dividers for obtaining the frequencies fb, fc and respective interruption signals INTERR(fb) and INTERR(fc) in synchrony with said frequencies.

The dividers mentioned are selected from among those commonly found in trade and are appropriately initialized with the values of K and N for the particular modulator implemented, after which the frequencies fb and fc are generated by dividing the main frequency by appropriate values derived from K and N.

The serial signal S_{in}(FIG. 1) reaches an input port PORTIN of the microprocessor and is loaded in shift register MEMSER under the control of the signal INTERR(fb). This signal times the beginning of a first cycle for acquisition of the input signal $S_{in}$and generation of the symbols Ii and Qi (FIG. 1).

The signal INTERR(fc) times a second cycle including processing of all the other phases of the modulation process including output. In the output phase a sample belonging to the modulated digital carrier QAM is transferred from an internal register BUFFEROUT, in which it is found, to an output port PORTOUT connected to the digital/analog converter DAC (FIG. 1).

More precisely, the sample present in BUFFEROUT is the one which among the samples Io, Qo, $\overline{\text{Io}}$, $\overline{\text{Qo}}$ (FIG. 1) has to be converted into analog.

With reference to FIGS. 3, 4 and 5 it is noted that the overall flow chart includes:

- an initialization phase INIZ shown in FIG. 3,
- the abovesaid first acquisition cycle of the signal S_{in}shown in FIG. 4 by the phases included between points A and A', and
- the abovesaid second cycle of modulation and output of the samples of the modulated digital carrier QAM shown in FIG. 5 by the phases included between points B and B'.

The two above-mentioned cycles are in practice two programmes for management of the respective interruption signals INTERR(fb) and INTERR(fc); the signal INTERR(fc) has priority over the signal INTERR-(fb) to avoid noise in the modulated carrier phases Sout.

The phase INIZ is performed only once at the start of the programme, after which the microprocessor waits for one or the other of the signals INTERR(fb) or INTERR(fc) to address the cycle of acquisition or modulation respectively.

The points A and A' represent the starting and ending addresses of the programme related to the acquisition cycle while the points B and B' represent the starting and ending addresses of the programme related to the modulation and output cycle.

In normal operation, upon arrival of the signal INTERR(fb) there is memorised in a special register the address of the modulation cycle instruction in the processing phase. After completion of the acquisition cycle the modulation cycle resumes exactly from the point of interruption.

Upon arrival of the signal INTERR(fc) the processing and output cycle starts as stated and at the end thereof the microprocessor goes into standby for the next signal INTERR(fc).

During the phase INIZ there are performed some initialization functions including among others zeroing of certain memory registers of the microprocessor used during processing. With reference to FIG. 3 it is noted that the following are zeroed:

- three indices indicated by NFLUS, NCAMP and CONT associated with an equal number of counters used for counting the number of bits per symbol, the number of samples per symbol and the number

of samples per period respectively of each in quadrature digital barrier;

- the shift register MEMSER which contains the bits of the input signal Sin;
- a register SIMB which contains the symbols obtained from Sin;
- two registers MEM.I and MEM.Q which contain the symbols Ii and Qi respectively derived from SIMB by the mapping operation;
- a register BUFFERCOEFF which contains the coefficients C1 ... Cp as in the array S1 of FIG. 2;
- two shift registers BUFFERIN.I and BUFFERIN.Q having a length of (M) words each and used respectively for memorising M symbols Ii and Qi corresponding with the symbols Do ... DM of any of the sequences S2 ... S6 of FIG. 2, and finally
- the register BUFFEROUT which contains the samples of the modulated digital carrier QAM Uo(t).

In relation to FIG. 4 the different phases are explained in detail as follows:

- Point A sends to phase A1 in which a bit of the input signal S_{in} is acquired from the input port PORTIN.
- In the subsequent phase A2 the bit of PORTIN is transferred to the left position of the shift register MEMSER.
- The index NBIT is then increased in phase A3.
- In phase A4 the value of NBIT is tested; if said value is less than the predetermined number N of bits per symbol, in phase A5 the bits of the register MEMSER are shifted right. At the end of phase A5 there is a return A' to the reentry point A for the delay of a new interruption signal INTERR(fb).
- If NBIT = N the contents of MEMSER are memorised in the register SIMB in phase A6.
- In the subsequent phase A7 the mapping operation for generation of the symbols Ii and Qi is performed.
- In phase A8 the index NBIT is zeroed, after which there is the delay A' to the point of reentry A for the delay of a new interruption signal INTERR(fb).

With reference to FIG. 5:

- Point B sends to phase B1 in which the contents of the output register BUFFEROUT are placed on the output port PORTOUT.
- In phase B2 the value of the NCAMP index is tested.
- If said value is less than K there is a jump to phase B6.
- If NCAMP is equal to K, in phase B3, a shift to the right of one position of the content of the shift registers BUFFERIN.I and BUFFERIN.Q is completed.
- In the subsequent phase B4 the symbols contained in the registers MEM.I and MEM.Q are transferred to the first position on the left of the registers BUFFERIN.I and BUFFERIN.Q respectively.
- In the subsequent phase B5 the NCAMP index is zeroed.
- In phase B6 the value of the CONT index is tested. The values 0, 1, 2 and 3 of CONT send to the phases B8, B9, B10 and B11 respectively in which the digital filtration of the symbols Ii and Qi is performed.

  The filtration operation is done by multiplying the symbols of the registers BUFFERIN.I and BUFFERIN.Q, identified by an index (d) by appropriate coefficients of the register BUFFERCOEFF, identified by an index (y), and adding the products obtained together.

  The index d undergoes unitary increases from 1 to M in a given interval T.

  The expression of the index y is as follows:

  $$y = K \times (d-1) + NCAMP + 1$$

  It allows placing the data Do ... DM belonging to the sequences S2 ... S6 of FIG. 2 in correspondence with the coefficients which in the array S1 are placed exactly above said data. This provides the dual advantage of avoiding operations whose products would be null and useless occupation of memory of the registers BUFFERIN.I and BUFFERIN.Q with words consisting of all zeros. The phases B8, B9, B10 and B11 are placed in chronological sequence; at each present time interval T the corresponding filtered symbols Io, Qo, $\bar{I}o$ and $\bar{Q}o$ are memorised in the register BUFFEROUT.
- The value 4 of the CONT index involves, in phase B7, zeroing of said index and return to phase B8 for cyclic repetition of the phases B8, B9, B10 and B11.
- Each of the phases B8, B9, B10 and B11 evolves in the same phase B12 in which the CONT and NCAMP indices are increased by one unit after which there is a return B' to point B for the delay of a new Interruption signal INTERR(fc).

Claims

1. Multi-level digital modulation process wherein a serial flow (S_{in}) having a bit frequency fb is parallelized forming first words of N bits called symbols (SIMB) having a symbol frequency fs from which are generated in synchronism second (Ii) and third words (Qi) belonging to a channel termed 'in phase' and a channel termed 'in quadrature' respectively, components along two orthogonal axes of a vector which digitally modulates a sinusoidal carrier both in phase and in amplitude (Vo(t)), characterized in that:

   said second and third words (Ii,Qi) having a symbol frequency fs are filtered digitally at a sampling frequency fc synchronous with said symbol frequency fs and corresponding to said symbol frequency fs multiplied by an appropriate number K greater than two;

   said sinusoidal carrier modulated digitally both in phase and amplitude (Vo(t)) has a frequency (fo) synchronous with said sampling frequency fc and equal to one fourth of said sampling frequency fc;

   said digital filtration comprises cycles divided in four time intervals corresponding to an equal number of consecutive periods of said sampling frequency fc, there being generated in an orderly manner in said cycles fourth (Io), fifth (Qo), sixth ($\overline{I}$o) and seventh ($\overline{Q}$o) words corresponding to said second ($\overline{I}$i) and third ($\overline{Q}$i) true filtered words and to said second (Ii) and third (Qi) negated filtered words respectively, considered in the associated time interval, and that

   said fourth (Io), fifth (Qo), sixth ($\overline{I}$o) and seventh ($\overline{Q}$o) words constitute discrete samples of said digitally modulated sinusoidal carrier (Vo(t)).

2. Multi-level digital modulation process in accordance with claim 1 characterized in that said digital filtration of said second and third words is of the transverse type with finite pulse response and consists:

   in a first of said four time intervals, of the multiplication of a first array (BUFFERCOEFF) comprising a number p of digital coefficients (C1 ... Cp), for a second sequence (BUFFERIN.I) comprising a number M of said second words (Ii) and the summation of all the products obtaining in correspondence said fourth words (Io);

   in a second of said four time intervals, of the multiplication of said first array (BUFFERCOEFF) for a third sequence (BUFFERIN.Q) comprising said number M of said third words (Qi) and summation of all the products obtaining in correspondence said fifth words (Qo);

   in a third of said four time intervals, of the multiplication of said first array (BUFFERCOEFF) by said second sequence (BUFFERIN.I), summation of all the products and negation of the result obtaining in correspondence said sixth words ($\overline{I}$o);

   in a fourth of said four time intervals, of multiplication of said first sequence (BUFFERCOEFF) by said third sequence (BUFFERIN.Q), summation of all the products and negation of the result obtaining in correspondence said seventh words ($\overline{Q}$o);

   said number of digital coefficients p being equal to the product of said number M of words belonging to said second or third sequence by said number K.

3. Multi-level digital modulation process in accordance with claim 2 characterized in that said multiplications of said first array (BUFFERCOEFF) by said second (BUFFERIN.I) and third (BUFFERIN.Q) sequences comprise M products of each of the words contained in the respective sequences multiplied by a corresponding coefficient (C1 ... C_p) belonging to said first array (BUFFERCOEFF), each word belonging to said second and third sequences being identified by values taken from a first index d varying from 1 to M by unitary increments in a given period of said frequency fc, and

   each said corresponding coefficient (C1 ... Cp) being identified by values taken from a second index y dependent on said first index d, on said number K and on the value of a third NCAMP index varying from zero to K by increments of one unit at each period of said frequency fc.

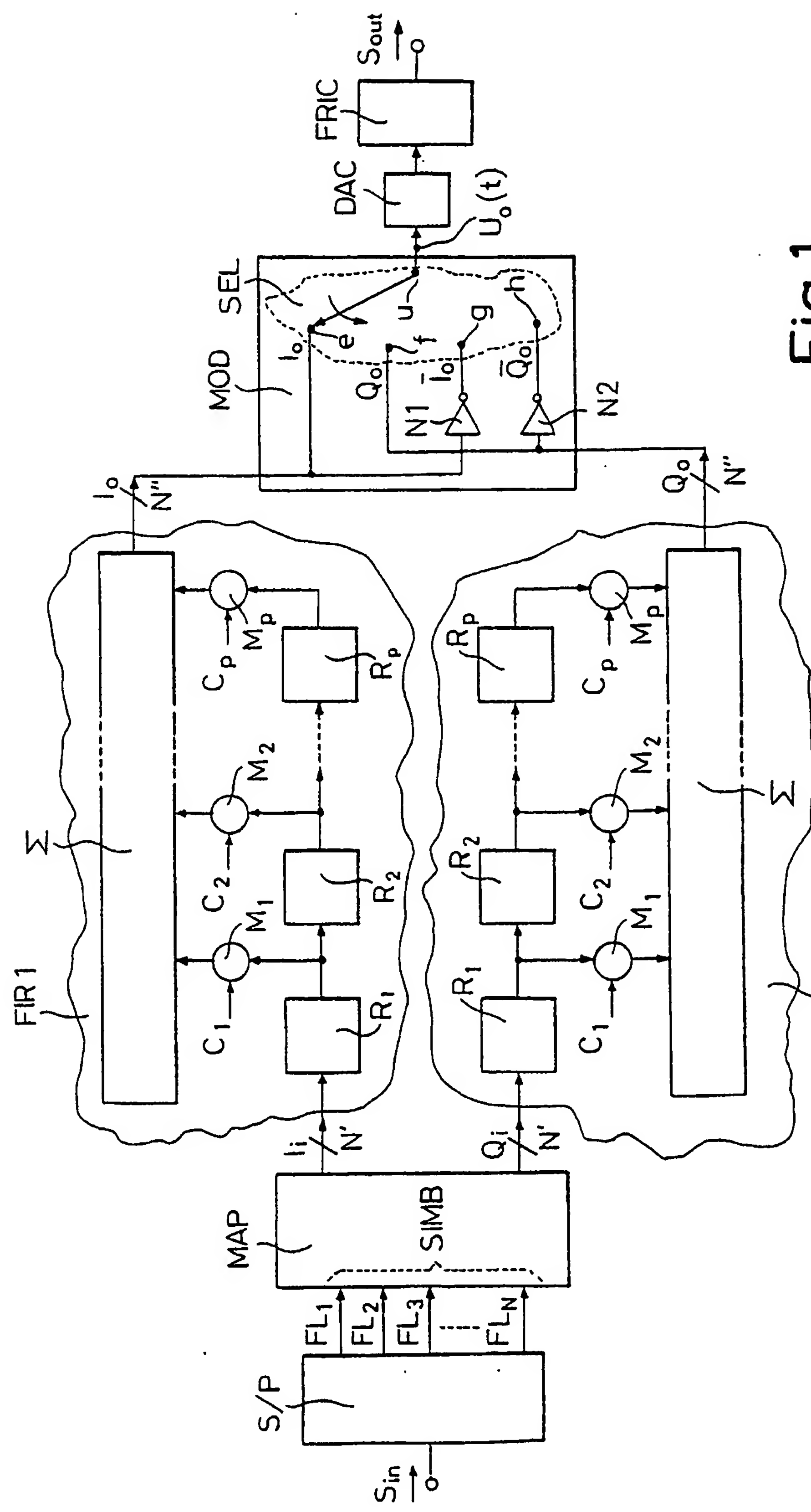
4. Multi-level digital modulation process in accordance with claim 3 characterized in that said index y has the following expression:

$$y = K \times (d-1) + NCAMP + 1$$

5. Multi-level digital modulation process in accordance with claim 2 characterized in that at each period of said symbol frequency (fs) all the words belonging to said second (BUFFERIN.I) and third (BUFFERIN.Q) sequences undergo a shift of one position without recovery.

6. Device for actuation of Multi-level digital modulation in accordance with the process of claim 1 characterized in that it is embodied by means of a single microprocessor designed for processing digital signals in real time.

7. Device for actuation of multi-level digital modulation in accordance with the process of claim 6 characterized in that it also comprises:
an oscillator circuit for the generation of a clock signal for timing the operation of said microprocessor,
a synchronization circuit for generation of one or more timing signals sent to said microprocessor for timing the input and parallelization phases of said serial flow (Sin) and the digital filtration and modulation phases,
a digital/analog converter (DAC) for conversion from digital to analog of said fourth (Io), fifth (Qo), sixth ($\bar{I}o$) and seventh ($\bar{Q}o$) words obtaining an equal number of discrete samples of said digitally modulated sinusoidal carrier (Vo(t)), and
a low-pass filter (FRIC) for filtering said discrete samples reconstructing said digitally modulated sinusoidal carrier (Sout).



S_{in}
S/P
FL_1
FL_2
FL_3
FL_N
MAP
SIMB
I_i
N'
Q_i
N'
FIR 1
C_1
M_1
R_1
C_2
M_2
R_2
C_p
M_p
R_p
Σ
FIR 2
C_1
M_1
R_1
C_2
M_2
R_2
C_p
M_p
R_p
Σ
I_o
N''
Q_o
N''
MOD
SEL
I_o
Q_o
$\bar{I}_o$
$\bar{Q}_o$
N1
N2
e
f
g
h
u
$u_o(t)$
DAC
FRIC
S_{out}

Fig.1

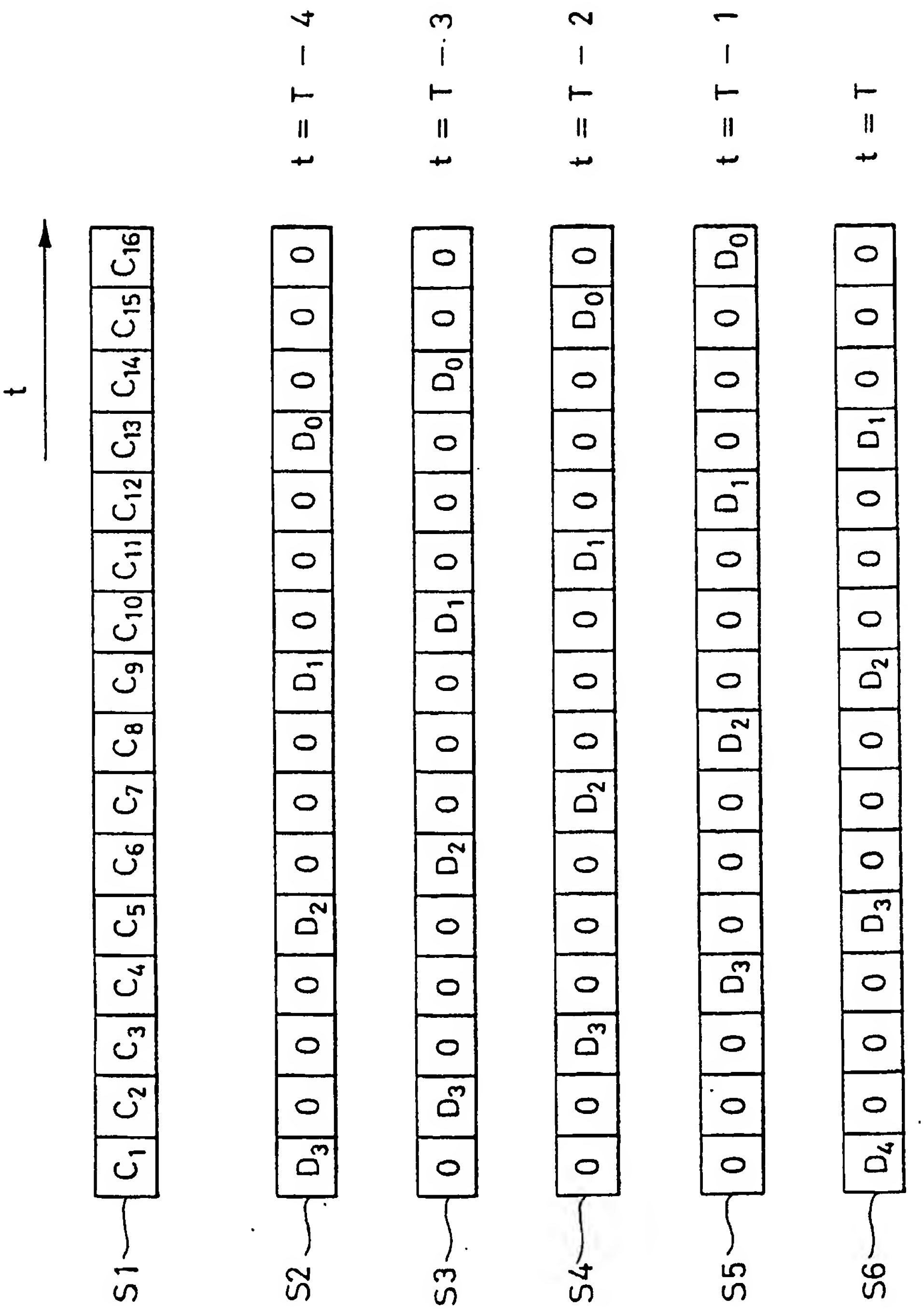


Fig.2

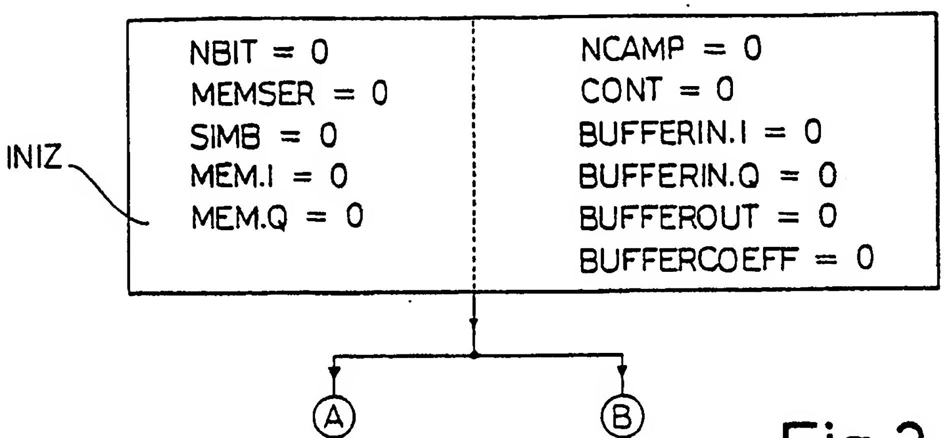

INIZ
NBIT = 0
MEMSER = 0
SIMB = 0
MEM.I = 0
MEM.Q = 0
NCAMP = 0
CONT = 0
BUFFERIN.I = 0
BUFFERIN.Q = 0
BUFFEROUT = 0
BUFFERCOEFF = 0
A
B

Fig.3

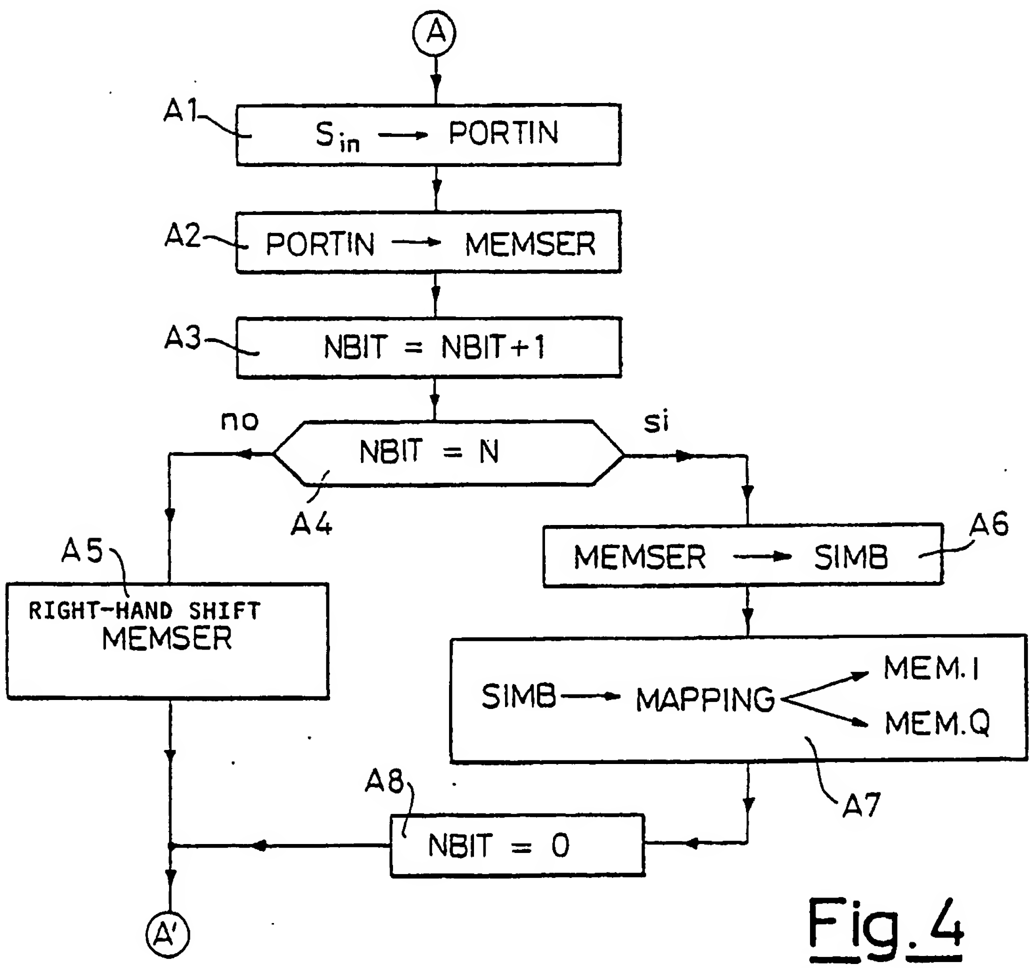

A
A1
Sin → PORTIN
A2
PORTIN → MEMSER
A3
NBIT = NBIT+1
no
si
NBIT = N
A4
A5
RIGHT-HAND SHIFT MEMSER
A6
MEMSER → SIMB
SIMB → MAPPING
MEM.I
MEM.Q
A7
A8
NBIT = 0
A'

Fig.4

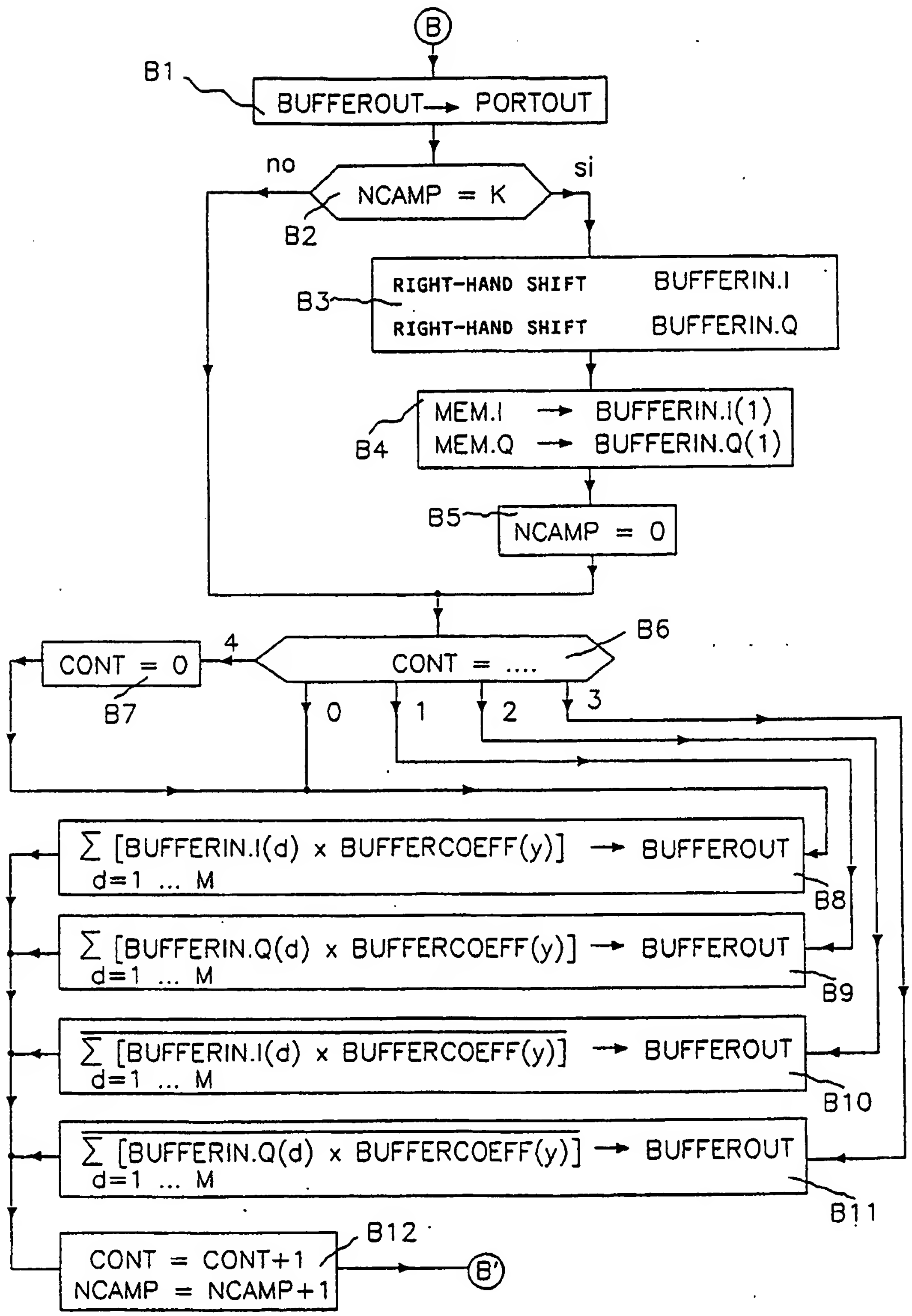

B
B1
BUFFEROUT → PORTOUT
no
si
NCAMP = K
B2
B3
RIGHT-HAND SHIFT BUFFERIN.I
RIGHT-HAND SHIFT BUFFERIN.Q
B4
MEM.I → BUFFERIN.I(1)
MEM.Q → BUFFERIN.Q(1)
B5
NCAMP = 0
B6
CONT = ...
4
0
1
2
3
CONT = 0
B7
Σ [BUFFERIN.I(d) x BUFFERCOEFF(y)] → BUFFEROUT
d=1 ... M
B8
Σ [BUFFERIN.Q(d) x BUFFERCOEFF(y)] → BUFFEROUT
d=1 ... M
B9
Σ [BUFFERIN.I(d) x BUFFERCOEFF(y)] → BUFFEROUT
d=1 ... M
B10
Σ [BUFFERIN.Q(d) x BUFFERCOEFF(y)] → BUFFEROUT
d=1 ... M
B11
CONT = CONT+1
NCAMP = NCAMP+1
B12
B'

FIG. 5